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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/627,057	07/25/2003	Yong Guen Lee	PIA30746/DBE/US	2208
36872 7590 08/21/2007 THE LAW OFFICES OF ANDREW D. FORTNEY, PH.D., P.C. 401 W FALLBROOK AVE STE 204 FRESNO, CA 93711-5835			EXAMINER WILCZEWSKI, MARY A	
			ART UNIT 2822	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

DETAILED ACTION

This Office action is in response to the Amendment and Request for Reconsideration filed on June 8, 2007.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1-10 and 15-23 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claim 1 has been amended to recite that ***all*** contact holes in the insulating layer over the active region are formed ***using a single pattern***. The originally-filed specification discloses that the insulating film is ***selectively patterned*** to form contact holes exposing the substrate and gate line, see ¶ [0019]. However, the specification does not provide support for claiming that ***all*** contact holes are formed ***using a single pattern***.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-10 and 15-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Park et al., US Patent 6,511,919, in view of Ishida, US Patent 6,642,555, both of record.

Park et al. disclose a method of forming self-aligned contact holes in an oxide layer by a method which comprises the steps of forming shallow trench isolation 102 to define an active region and an element isolation region in a semiconductor substrate 100 (column 5, lines 3-6); forming a plurality of gate lines 104 within the active region, the plurality of gate lines not extending over a center of the trench (column 5, lines 21-26, and figure 4A); forming an insulating layer 108 on the plurality of gate lines 104 and the substrate 100 (column 5, lines 38-44, and figure 4C); forming contact holes in insulating layer 108 over an active region using a single pattern (column 5, lines 44-46), wherein a first group of the contact holes 110c that exposes portions of the gate lines (that is, exposes nitride spacers 106) and a second group of the contact holes 110d that exposes portions of the substrate in the active region (column 5, lines 45-55, and figure 4D); and forming contact plugs 112c, 112d in each of the plurality of contact holes (column 6, lines 4-8 and figure 4E). Park et al. lack anticipation only of forming a

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conductive pattern layer over the insulating layer that is electrically connected with the contact plug.

Ishida discloses a method of fabricating an SRAM cell as shown in figures 6A, 6B, and 6C, in which a conductive pattern layer is electrically connected with the contact plug. As shown in figure 6A, the gate lines are not connected with each other in the element isolation region and connections to the gate lines are made in the active region. In light of the disclosure of Ishida, it would have been obvious to one skilled in the art to form a conductive pattern layer that is electrically connected with the contact plug in order to make contact the gate lines and to fabricate an operable device. The thickness of the conductive pattern layer (claim 5) would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose this particular thickness, since Applicant has not disclosed that this thickness is for a particular unobvious purpose, produces an unexpected result, or is otherwise critical, and it appears prima facie that the process would possess utility using another thickness. Moreover, it has been held that limitations directed to size and configuration are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, *In re Rose*, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); *In re Rinehart*, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); *Gardner v. TEC Systems, Inc.*, 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert.

denied, 469 U.S. 830, 225 USPQ 232 (1984); *In re Dailey*, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

Response to Arguments

Applicant's arguments filed June 8, 2007, have been fully considered but they are not persuasive. Applicant has argued that since the contact holes 110 of Park do not expose the gate lines 104, which remain covered by nitride spacers 106 (see, e.g., 4D-4E), Park fails to disclose forming contact holes in an insulating layer over an active region, wherein a first group of the contact holes exposes portions of gate lines and a second group of the contact holes exposes portions of a substrate in the active region, as recited in Claim 1. First, claim 1 ***does not*** require that the contact holes are formed to ***expose*** the gate lines. Claim 1 only requires that the contact holes expose ***portions*** of the gate lines. Second, the nitride spacers 106 covering the gate lines 104 in the known method of Park are clearly a ***portion*** of the gate lines. As shown in Figure 4D, Park discloses forming contact holes in insulating layer 108 over an active region, wherein a first group of contact holes 110c exposes portions of gate lines (that is, exposes nitride spacers 106) and a second group of the contact holes 110d exposes portions of the substrate in the active region, as required in Claim 1.

Allowable Subject Matter

Claims 21-23 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to M. Wilczewski whose telephone number is (571) 272-1849. The examiner can normally be reached on Monday and Thursday.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on 571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



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